

IEEE ICC 2017 21-25 May 2017 // Paris, France





Workshop on Channel Coding for 5G and Future Networks

Channel coding is a well-studied subject – some say. The challenges faced by the code design for future networks, however, clearly falsifies this statement. 5G, as an example for a wireless network, requires coding schemes that cover large ranges of code lengths and code rates. Optical communications, as an example for a wired network, requires extremely low error rates. For both examples, low decoding complexity, low decoding latency and high hardware efficiency are mandatory.

Turbo codes, low-density parity check codes and polar codes are among the most promising candidates. While all these codes are capacity approaching, each class of codes has their own advantages and disadvantages at practical code lengths. This is particularly true with respect to the challenging requirements of future networks. Code design and decoder architectures for these code classes are also in different states of development and practical implementation. A few examples: turbo codes are very well developed with respect to their decoder implementation but they typically exhibit error floors; LDPC codes are very efficient at high code rates but design for low code rates is difficult; polar codes can deal with a large range of rates but their decoding latency is potentially high.

This workshop aims at presenting the state-of-the-art in modern channel coding and solutions to address channel coding problems expected in future networks. For providing the full picture, the topics range from coding theory over code design and decoder design to implementation aspects.

The workshop will provide a platform for the dissemination of research on topics of interest but not limited to the following:

- Polar code designs
- Advanced LDPC codes
- Structural properties of polar codes and LDPC codes
- Techniques and designs for length and rate adaptation
- Techniques and designs for HARQ
- Coding for higher-order modulation
- Decoding architectures
- Efficient hardware implementation

Important Dates

Paper Submission: 18 November 2016 Notification Date: 17 February 2017 Final Paper: 10 March 2017

Organizing Committee

General Chairs

Ingmar Land, Huawei Paris, France Jean-Claude Belfiore, Huawei Paris, France Program Chairs

Emanuele Viterbo, Monash University, Melbourne, Australia David Declercq, Université Cergy-Pontoise, France Emmanuel Boutillon, Université de Bretagne Sud, France